Comparison of Alternative Approaches to High-Power Thin-Film LED Chip Design

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Abstract – *Vertical and planar thin-film flip-chip blue LEDs are compared by simulation to identify strong and weak points of approaches to their design. Current crowding and its effect on internal quantum efficiency and light extraction efficiency are found to be key factors limiting the device performance.*

Thin-film flip-chip (TFFC) design of III-nitride LEDs based on substrate removal after growth of device heterostructure followed by texturing the back side of the n-GaN contact layer has been suggested for substantial improvement of light extraction efficiency from the LED die [1-3]. Currently two alternative approaches are employed in the LED industry. One utilizes the vertical current injection, having contact electrodes formed on the n-GaN surface extracting the emitted light [1-2]. Another approach uses on-one-side (planar) electrode configuration with the n-electrodes contacting the n-GaN layer via holes etched through the p-contact layer and active region of the LED structure [3]. Despite a wide practical application of these approaches, their strong and weak points are not yet completely understood.

This paper reports on simulation analysis aimed at a better understanding of TFFC LED operation and comparing performances of vertical and planar LED dice. Essential point of the analysis is the consideration of identical LED heterostructures and key elements of the chip design, like texture formed on the n-GaN back surface, for every type of the die. This enables a more informative comparison of the LED characteristics.

The LED structure consists of a thick n-GaN contact layer with electron concentration $n = 1.5\times10^{18}$ cm^{-3}, an active region, a 40 nm p-Al$_{0.2}$Ga$_{0.8}$N electron blocking layer, and a 200 nm p-GaN contact layer with Mg concentration of 2.5×10^{19} cm^{-3}. The active region contains four 3 nm InGaN quantum wells (QWs) emitting light at 452 nm separated by 10 nm unintentionally doped GaN barriers ($n = 5\times10^{16}$ cm^{-3}). Designs of 815×875 μm^2 vertical and 1000×1000 μm^2 planar dice are shown schematically in Figs.1a and 1b, respectively. The thickness of the n-GaN contact layer is of 3 μm in the vertical die and 5 μm in the planar one. The thermal resistances of the vertical and planar dice mounted on a heat sink are set to be of 8.2 and 9.5 K/W, respectively.
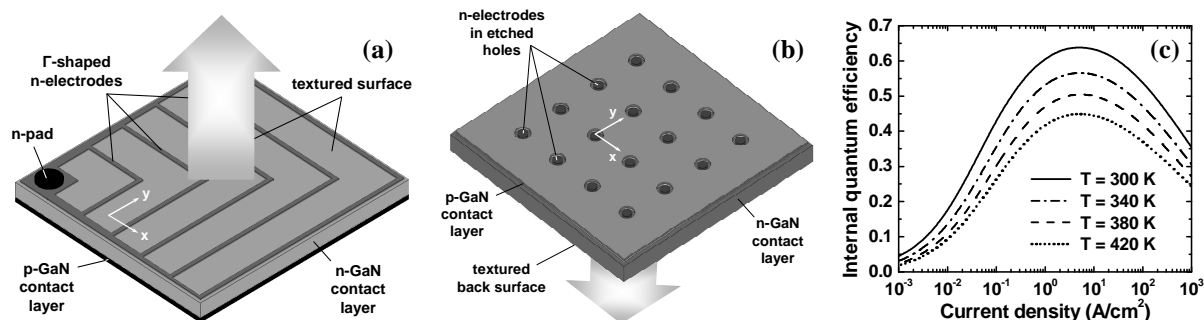

Fig.1 Schematic vertical (a) and planar (a) TFFC dice; arrows indicate the main directions of light emission. IQE of the LED structure *versus* current density computed for various temperatures (c).

Modeling of the LED operation is performed with commercial SimuLED package [4] providing coupled 3D analysis of electrical, thermal, and optical processes in the LED dice. Auger recombination in InGaN QWs is accounted for as a principal mechanism limiting the internal quantum efficiency (IQE) of LED structures at high-current densities [5,6] – see Fig.1c. The texturing of the n-contact layer surface was simulated via close-packed array of hexagonal pyramids having the period of 500 nm and height-to-base ratio of about four. Optical properties of gold and silver were used in the 3D ray-tracing analysis for the n- and p-electrodes, respectively.

Simulations predict a strong current crowding near the n-electrode edges in both vertical and planar dice (Figs.2a and 2b). The higher the total current flowing through the LED, the stronger is the current density non-uniformity in the active region. Because of a smaller total perimeter of the n-electrodes, the crowding is much more pronounced in the planar die, resulting, in particular, in a higher operation voltage at high-current operation (Fig.2c). In the vertical die, the current density peaks under the n-pad and, to a lesser extent, under the Γ-shaped electrodes (Fig.2a). The light emitted in these regions has much lower probability of extraction from the die, owing to optical losses caused by incomplete light reflection from metallic n-electrodes (Fig.3a). As a

result, the light extraction efficiency (LEE) of the vertical TFFC LED becomes current-dependent (Fig.3b). The decay of LEE with current can be considerably reduced by inserting an insulation layer under the n-pad and using narrower Γ-shaped electrodes with a smaller interelectrode spacing (improved design of the vertical chip). In contrast, LEE of the planar LED does not practically vary with current and exceeds that of the vertical LED due to the absence of n-electrodes on the emitting n-GaN surface. However, such a die exhibits a stronger IQE droop related to a much higher current localization next to the n-electrode edges. All the above effects determine the variation of the LED wall-plug efficiency (WPE) with current specific for every type of the die (see Fig.3c).
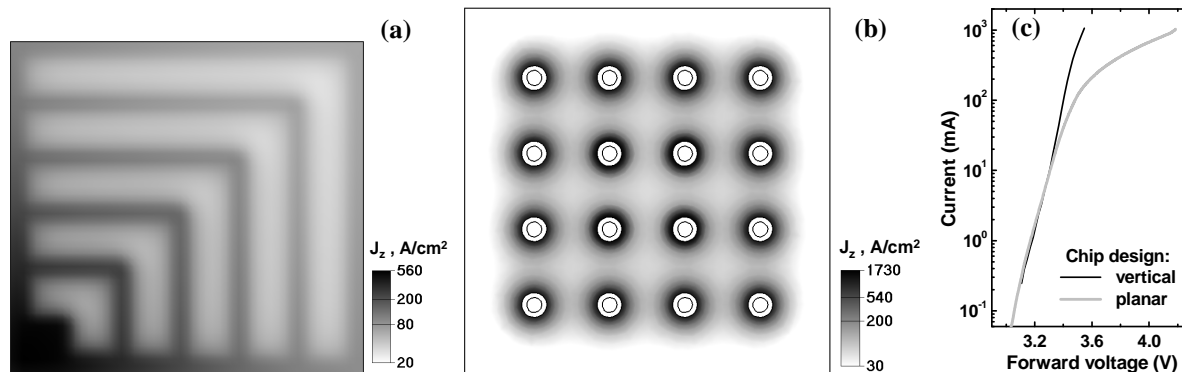
Fig.2 Current density distribution in the active region of (a) vertical die at 700 mA and (b) planar die at 960 mA; in both cases, the mean current density is of ~96 A/cm^2. Current-voltage characteristics of the dice (c).
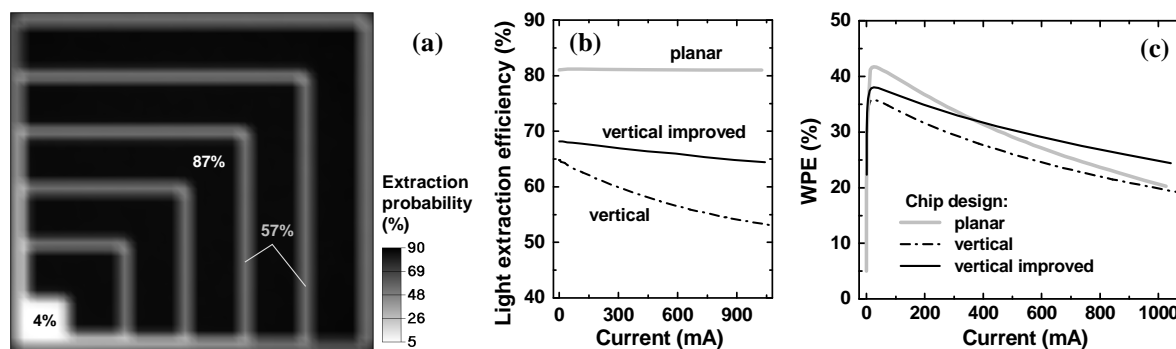
Fig.3 Probability of light extraction from a certain point of active region in the vertical die (a). Light extraction efficiency (b) and wall-plug efficiency (c) of the planar and vertical dice as a function of current.

Actually, two types of the die considered above imply different strategies of further development. The vertical die primarily requires improvement of LEE that can be accomplished by optimization of the chip design, i.e. by modification of the n-electrode geometry, using current blocking layers, etc. The performance of the planar LEDs, however, may be improved at the expense of the heterostructure optimization aimed at increasing its IQE at high current densities (see [7], as an example of such an optimization).

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