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Investigation of the p-GaN Ohmic Contact Property by Using a Synchrotron Radiation Analysis

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We report the optimized process and Ohmic mechanism for an indium tin oxide (ITO)/p-GaN Ohmic contact. The current transfer enhanced layer (CTEL) on the top of p-type GaN was introduced to improve the Ohmic properties. The samples were annealed at temperatures in the range of 400 ∼ 800 °C under gas ambients of 0 (*i.e.*, pure N_2), 0.1, 0.2, and 0.5 % O_2/N_2 ratio. A small amount of O_2 addition shows much lower contact resistance than the pure N_2 only ambient while a high O_2/N_2 ratio exhibits an abruptly increasing the contact resistance and operating voltage. The contact resistance of the ITO/(CTEL)/p-GaN layer shows the best value of 1.43×10^{-3} ohm·cm^2 at the annealing temperature of 650 °C and a 0.1 % O_2/N_2 gas ambient. High resolution near edge X-ray absorption spectroscopy (NEXAFS) shows that more interstitial N_2 molecules were formed from the ITO/CTEL interfaces with increasing O_2/N_2 ratio. From the NEXAFS results, the high contact resistance could be explained with a possible reaction, $2GaN + 3/2O_2 \rightarrow Ga_2O_3 + N_2$, during the annealing process. It could be suggested that the newly formed oxide layer makes the depletion width more narrowing for the Ohmic contact with a tunneling junction. However, the thick oxide layer formed at the high O_2/N_2 ratio might keep the hole carriers from transporting to the electrode.

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I. INTRODUCTION

GaN (III-V) compounds have attracted much attention for their use in light-emitting diodes (LEDs), laser diodes (LDs), photodetectors (PDs), solid state lighting divices, and full color display devices [1,2]. One of the major concerns in the fabrication of LEDs is that the p-GaN has poor electrical properties due to its very low carrier concentration ($\sim \times 10^{17}$ Mg/cm^3), large acceptor ionization energy (∼170 meV or higher), and large work function (Φ = 7.5 eV) [3]. The poor electrical properties in the contact interface cause the device to have a lower thermal stability and reliability when the operating voltage is raised. The major loss of device performance is related to the Ohmic contact property.

Many studies have been reported the preparation of a low resistance electrode by combining various metals, such as Pt/Au, Ti/Pt/Au, Pt/Au, Ni/Cr/Au, Pd/Au, and Ni/Au [4–7]. Among them, the Ni/Au electrode was commercialized owing to its having the lowest specific electrical resistance of 2.7×10^{-4} ohm·cm^2. Kim *et al.* showed that the specific contact resistance of the semi-transparent Ni(2 nm)/Au(3 nm)/ITO(60 nm) system was 8.8×10^{-4} ohm·cm^2 [8]. This system was annealed at a temperature of 500 °C in an O_2 ambient. It was recommended that pre-annealing of the Ni/Au before the ITO deposition led to a better contact resistance value of 2.2×10^{-4} ohm·cm^2. Horng *et al.* investi-

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gated the Ohmic property of a Ni(10 nm)/ITO(250 nm) bilayer system [9]. The as-prepared electrode showed Schottky characteristics; on the other hand, the rapid thermal processed one revealed a low resistance of 8.6×10^{-4} ohm·cm^2 at a temperature of 600 °C in an air atmosphere. It was suggested that the contact resistance was lowered by an increase in the of hole carrier concentration, and that a p-type semiconductor NiO had been formed at the interface.

However, the external efficiency declines by less than 50 % transmittance of the metal electrode in the visible region in spite of its having a good electrical property. Among the transparent conductive oxides, such as indium tin oxide (ITO), aluminum-doped zinc oxide (AZO), indium zinc oxide (IZO) and cadmium tin oxide (CTO), ITO is a good candidate material to replace the semi-transparent metal electrode, because the transmittance is more than 95 % and because it has good electrical properties, such as low resistance (5×10^{-4} °C), high carrier concentration ($10^{20} \sim 10^{21}$/cm^3) and mobility (20 $\sim$ 25 cm^2/V·S) [10–12]. The light extraction efficiency is expected to increase to more than 10 % if the metal electrode is used for ITO. When the ITO is directly deposited on the p-GaN semiconductor, the electrical property is non-Ohmic. Therefore, a new process development is needed to optimize the Ohmic contact property. Chang *et al.* reported that a thin $In_{0.1}Ga_{0.9}N$ layer inserted into the ITO/p-GaN interface reduced the Schottky barrier height [13]. The contact resistance was 4.5×10^{-2} ohm·cm^2 after annealing at a temperature of 500 °C in a N_2 environment. They suggested that Ga-vacancies created by out-diffusion of gallium atoms played an important role in the Ohmic mechanism. Kuo *et al.* reported that the low resistance (1.2×10^{-3} ohm·cm^2) and a high transmittance (86.5 %) had been attained by inserting a Si-doped n$^+$ InGaN/GaN short-period superlattice (SPS) layer [14]. This layer was functioned as a tunneling layer.

According to the previous results, there is a tendency to adopt a high-transmittance electrode like ITO rather than a semi-transparent metal electrode, although metal electrode shows better electrical properties than ITO does. However, few works in the literature have addressed currently available processes and the mechanism of Ohmic contact, although many studies have been performed to improve the ITO/p-GaN Ohmic characteristics [15,16]. In this study, we report optimized results for the Ohmic properties by inserting a charge transport enhanced layer (CTEL), on n$^+$ InGaN/GaN superlattice. We also suggest the Ohmic mechanism between the p-GaN/CTEL and the ITO layer by using a surface analysis and a synchrotron radiation analysis.

II. EXPERIMENT

The epitaxial layer of the LED structure was grown on a sapphire substrate the using metal-organic chemical vapor deposition (MOCVD). The LED structure is as follows: a GaN nucleation layer deposited at 520 °C, a 3 μm-thick Si-doped GaN layer, a five period InGaN/GaN multiple quantum well (MQW), and a 0.15 μm-thick Mg doped GaN layer. The Mg doping concentration of p-GaN was 1.2×10^{20}/cm^3. The charge transfer enhanced layer (CTEL) deposited on p-GaN was a Si-doped InGaN/GaN superlattice with a the because of several nm. The ITO electrode was deposited by using the R.F.-magnetron sputtering method and had a thickness of 300 nm. The electrical properties were measured at various annealing conditions for the ITO(30 nm)/CTEL(n$^+$ InGaN/GaN)/p$^-$GaN sample. The operation voltages (Vop) were measured at 20 mA with a 375×330 μm^2 lateral structure LED. The contact resistances were calculated using the circular-TLM method.

ITO samples of 5 nm in thickness were specially designed to study the chemistry of interface reaction because it is impossible to investigate non-destructively the interface by inserting a CTEL overlayer as thick as 300 nm. These samples were annealed at temperatures of (400 °C, 650 °C, and 800 °C) in (pure N_2, 0.1 % O_2/N_2, 0.2 % O_2/N_2, and 0.5 % O_2/N_2). Surface and interface analyses for the annealed samples were performed using X-ray photoelectron spectroscopy (XPS), time-of-flight secondary ion mass spectrometry (TOF-SIMS), scanning electron microscopy (SEM), and atomic force microscopy (AFM). Near-edge X-ray absorption spectroscopy (NEXAFS) was also utilized to analyze the chemical species newly formed at the interface. The NEXAFS experiment was conducted at the 8A1(U7) beam line in the Pohang Accelerator Laboratory (PAL). The spectra were obtained by recording the sample current in total electron yield (TEY) mode as a function of energy. The absolute photon energy scale was referenced to the value of 401.10 eV, which position is the second π^* resonance peak for gas phase N_2.

III. RESULTS AND DISCUSSION

Figure 1 shows the operation voltages (Vop) and contact resistances at a temperature of 650 °C for various ambient conditions (pure N_2, 0.1 % O_2/N_2, 0.2 % O_2/N_2, and 0.5 % O_2/N_2). The operation voltage (Vop) and the contact resistance are 3.38 V and 4×10^{-2} ohm·cm^2, respectively, for pure N_2, reach their lowest values of 3.27 V and 1.43×10^{-3} ohm·cm^2 at a 0.1 % O_2/N_2 ratio, and finally rise again to 3.53 V and 3.1×10^{-1} ohm·cm^2 with increasing rate of O_2/N_2 ratio. It is noted that the addition of O_2 is undoubtedly required to achieve the optimum Ohmic condition during the annealing process; however, a large amount of O_2 can bring about a bad effect.

Figure 2 shows the high-resolution N K-edge NEXAFS spectra for various conditions. As mentioned above, the NEXAFS technique is able to examine the interface reaction non-destructively, unlike XPS, SIMS, and AES

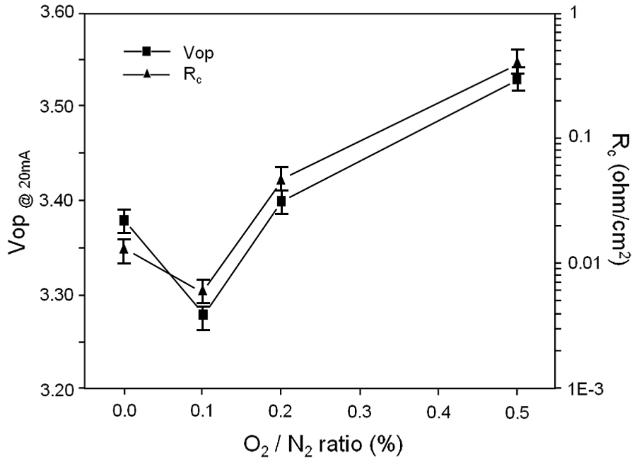

Fig. 1. Electrical properties of the ITO electrode contacting CTEL/p-GaN annealed with O_2/N_2 % as a functional of the O_2/N_2 % ratio at 650 °C: filled squares: Vop and triangle: R_c.

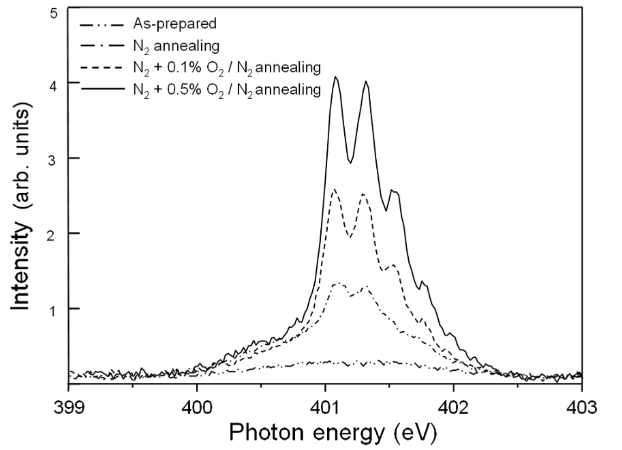

Fig. 2. High-resolution N K-edge NEXAFS spectra of ITO electrode annealed at several O_2/N_2 % ratios at 650 °C.

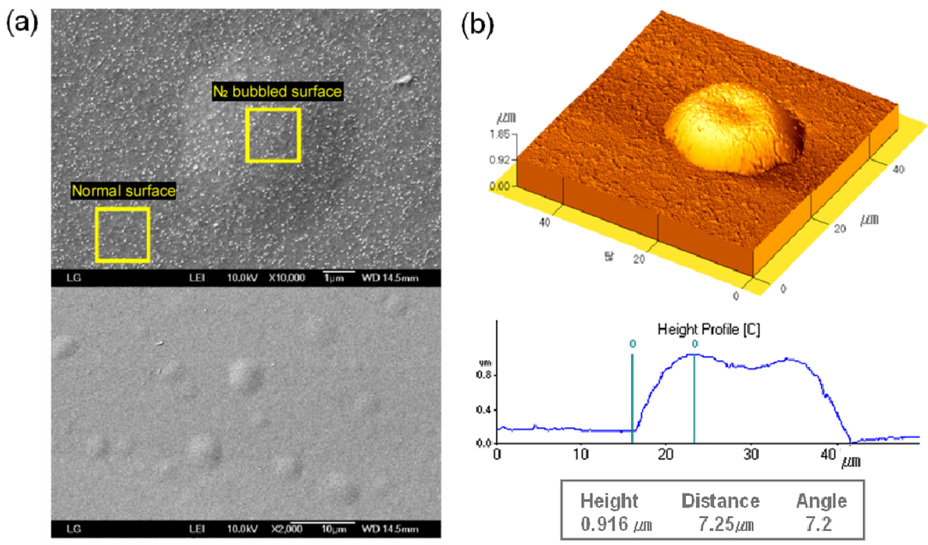

Fig. 3. SEM micrograph and AFM topography image for a severely annealed ITO electrode (a) SEM Micrography (b) AFM Topography.

analyses. The optimum thickness of the ITO overlayer was chosen by the highest N K-edge intensity among the 5 nm, 10 nm, 30 nm thicknesses. Then, NEXAFS data were obtained from the ITO thickness of 5 nm. Although it is still controversial whether the N K-edge spectrum is due to either atomic nitrogen or interstitial molecular N_2, it has been concluded that the split high resolution spectrum, N1s→ π^* orbital transition, originates from the vibrational structure of N_2 molecules because this transition did not occur in the pre-annealing sample, the as-prepared one in dash-dot-dot line of the Figure 2. Similar results were also published in the previous study on the SiON thin film [17]. In the N K-edge spectra, the molecular N_2 intensity increased in proportion to the O_2 amount. This indicates that addition of O_2 during the annealing is essential to optimize the electrical properties however, an increasing amount of O_2 does not always favor the contact resistance. That is, the electrical property shows an increasing tendency after an initial decrease unlike the O_2 intensity. Though not shown in this study, the molecular N_2 intensity increased with increasing temperature from 400 °C to 800 °C in a 0.1 % O_2/N_2 ambient. There was no N_2 generation at the lowest annealing temperature of 400 °C, irrespective of the O_2 amount, however, the N_2 generation at occurred annealing temperatures of 650 °C and 800 °C and increased with increasing amount of O_2. This indicates that generation of N_2 gas can cause Ga-vacancies, which are created by out-diffusion of gallium atoms through the CTEL tunneling layer, resulting in a decrease in the electrical resistance of up to 1.2×10^{-3} ohm·cm^2) between a 0 % and a 0.1 % O_2/N_2 ambient.

Figure 3 shows AFM and SEM micrograph images of a severely annealed surface at a high temperature (800 °C) for 1 hr. Bubbles that formed at the interface between ITO and p-GaN are observed in the picture. The harsh annealing condition leads to much more generation of N_2 gas. Then, the interface gets loose and the electrical property declines due to a reduction of the contact area, and device failure is induced by a local thermal effect.

From the above results, the Ohmic mechanism can be considered from a correlation between the evolution quantity of N_2 and the electrical properties. A chemical reaction equation for N_2 evolution can be proposed as below:

$$2\mathrm{GaN} + 3/2\mathrm{O_2} \rightarrow \mathrm{Ga_2O_3} + \mathrm{N_2} \qquad (1)$$

The Gibbs free energies of the GaN and the Ga_2O_3 compounds are −118.5 kJ/mol and −998.3 kJ/mol, respectively [18]. Since oxide is more thermodynamically stable than nitride, the direction of this reaction tends to the right. According to Eq. (1), the molecular N_2 observed in the NEXAFS spectrum would be produced by decomposition of GaN at a moderate condition, 650 °C and 0.1 % O_2/N_2. Then, hole transport might be expedited by tunneling through the thin oxide layer. However, a thickly formed Ga_2O_3 layer prevents hole carriers from transporting to the ITO electrode, and a large amount of N_2 can result in bubbling, which degrade the contact interface under severe annealing conditions, as already shown in Figure 3. This explains sufficiently the relation of annealing conditions and electrical properties. It is also indicates that we have to search for the optimum range of the process window to achieve the lowest operating voltage and contact resistance.

It is known that inserting an insulating buffer layer enhances the tunneling property. Similar studies have examined the role of an insulating layer at the interface in organic light emitting diodes [19, 20]. The reason is that dipolar electrostatic charges of ionic bonding are polarized at the interface between ITO (anode, hole injection) and a p-type semiconductor and the distribution of a dipolar layer helps the depletion width to narrow for Ohmic contact. The injection barrier height is, thus, reduced.

IV. SUMMARY

The optimized process for a indium-tin oxide (ITO)/p-GaN Ohmic contact has been studied. The current transfer enhanced layer (CTEL) was deposited on top of p-type GaN to reduce the Schottky barrier height. This was annealed under the various annealing conditions to improve the electrical property. The contact resistance of the ITO/p-GaN layer had its lowest value of 1.43×10^{-3} ohm·cm^2 at a temperature of 650 °C and a 0.1 % O_2/N_2 ratio ambient. High-resolution near-edge X-ray absorption spectroscopy (NEXAFS) and other surface analytical techniques were used to investigate the reaction of the contact layer. The NEXAFS technique has a merit in observing the interface non-destructively and directly observed the vibrationally resolved N K-edge absorption spectra at the contact interface. We proposed that the molecular N_2 would be formed from the reaction equation, $2GaN + 3/2O_2 \rightarrow Ga_2O_3 + N_2$, during the annealing process. The evolution of N_2 increases with increasing O_2/N_2 % ratio and annealing temperature. The relation between the electrical property and the annealing process was examined. It could be suggested that the newly formed oxide layer narrowed the depletion width for Ohmic contact with tunneling junction. However, a thick oxide layer and a large amount of N_2 evolution might prevent hole carriers from transporting to the electrode.

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