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Comparison of alternative approaches to high-power thin-film LED chip design

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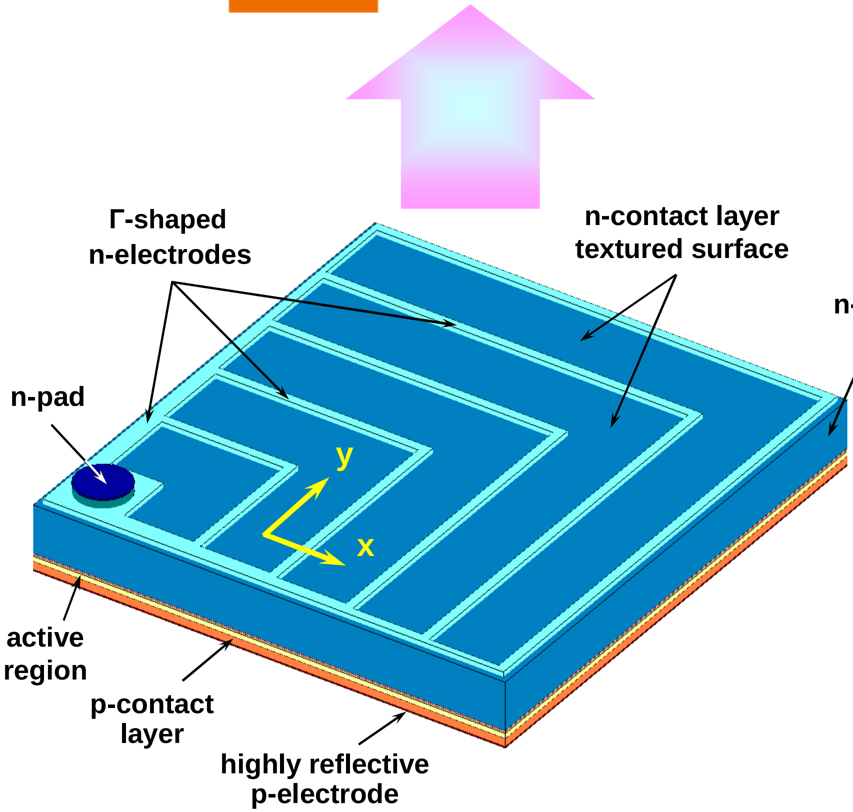
Vertical and planar LED dice with removed substrates

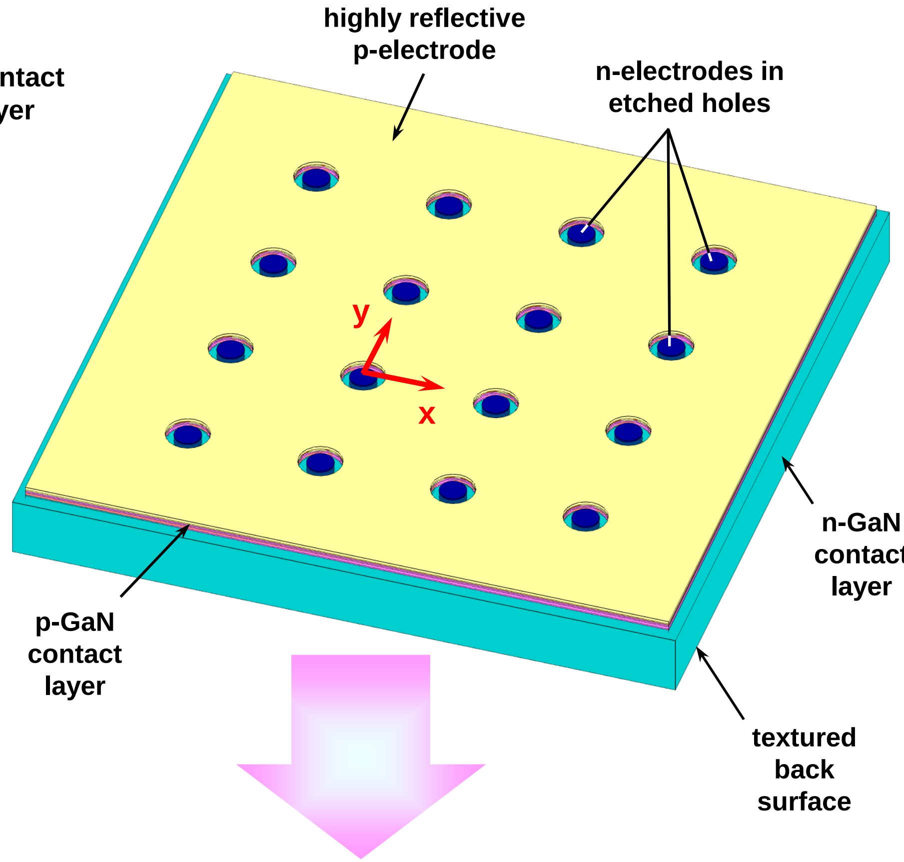


815×875 vertical LED die

V. Härle et al., Proc. SPIE 4996 (2003) 133; phys. stat. solidi (a) 201 (2004) 2736

O. Shchekin et al., Appl. Phys. Lett. 89 (2006) 071109

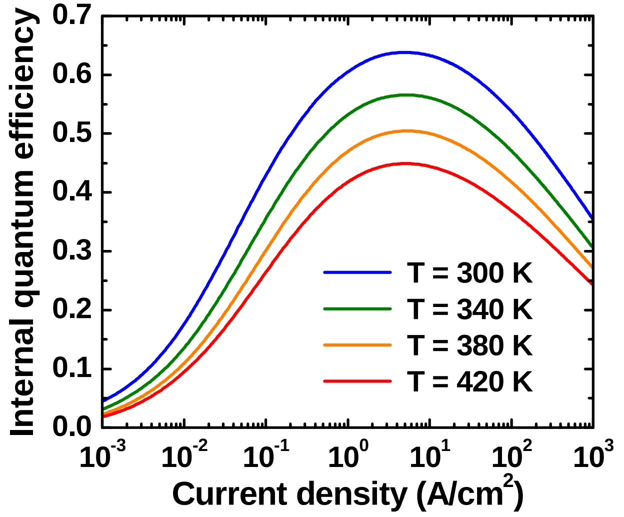
1000×1000 planar LED die



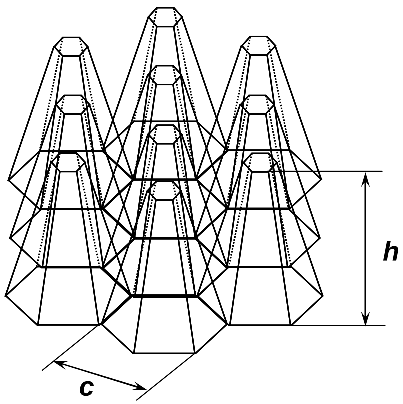
Key elements of simulation model

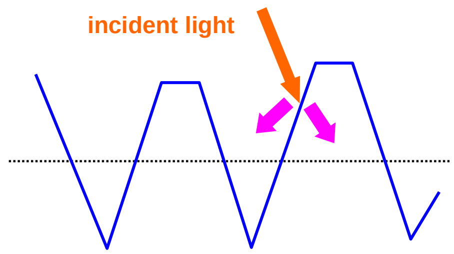
SimuLED™ package is used for modeling:
http://www.str-soft.com/products/SimuLED

- 3D coupled simulation of electrical, thermal, and optical processes in the LED die
- Auger recombination is considered is the main non-thermal mechanism of the IQE droop at high current densities
- textured surface is modeled by closely packed hexagonal pyramids with the aspect ratio *h/c* ~ 4
- optical properties of Au and Ag are used for n- and high-reflective p-electrodes, respectively



no electron leakage is predicted for InGaN MQW LED structure

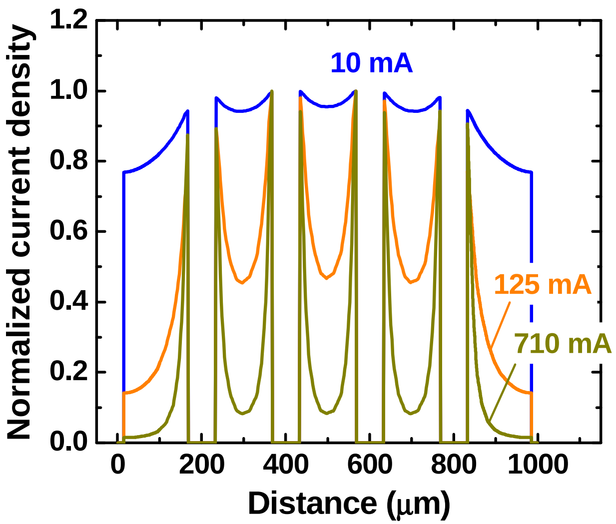


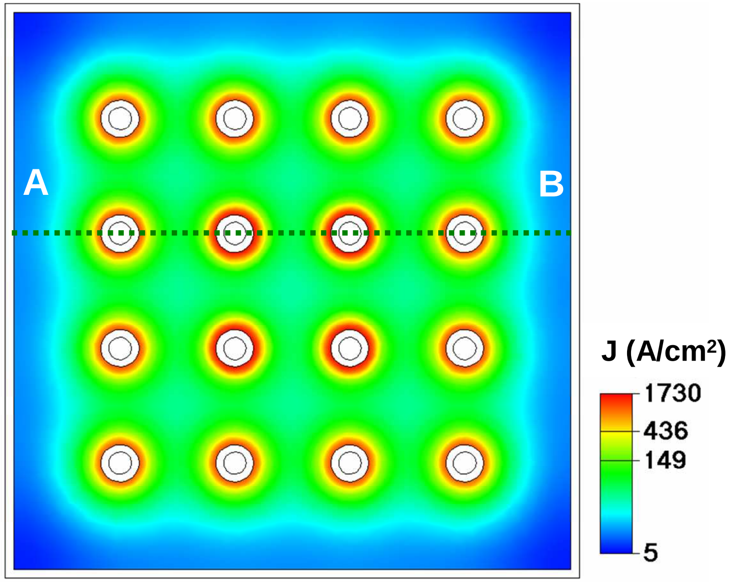


Current crowding in the active region

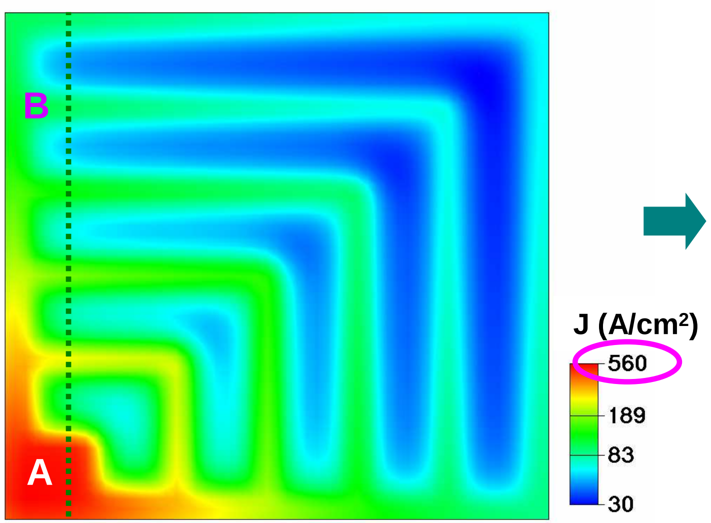
The mean current density in both dice is ~ 96 A/cm²

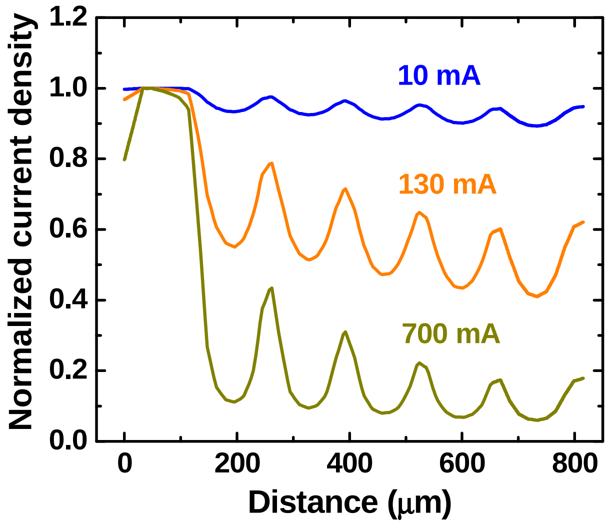
I = 960 mA





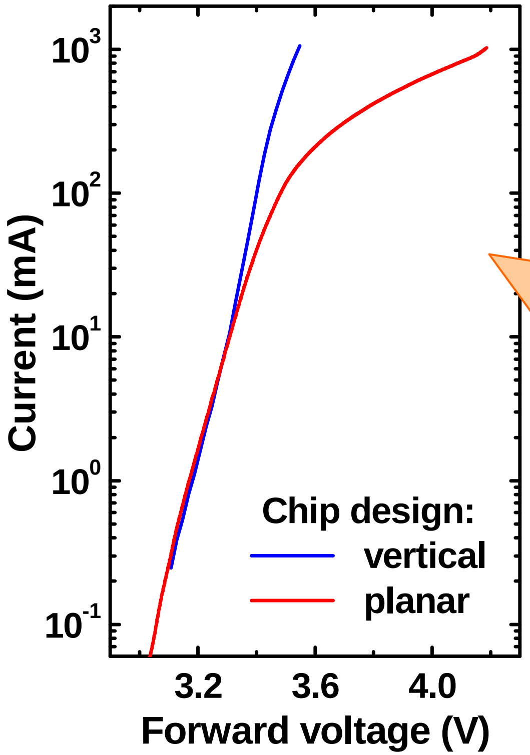
I = 700 mA





current density non-uniformity depends on the total operating current

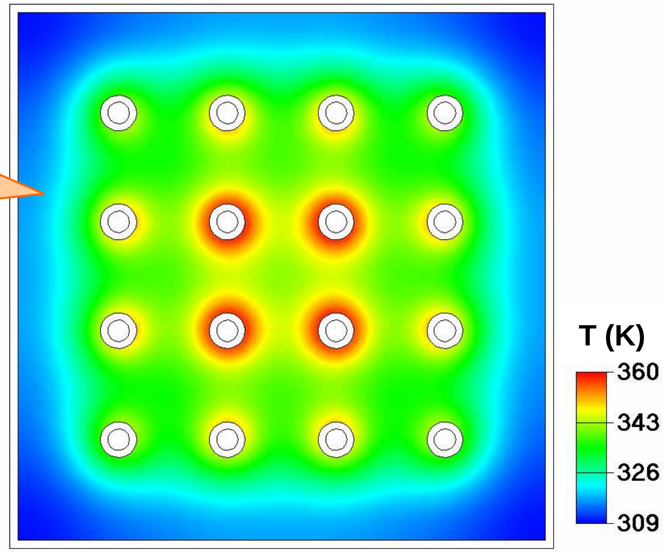
Current crowding effect on local overheating and I-V curves



a higher series resistance of the planar LED caused by a smaller total n-electrode perimeter

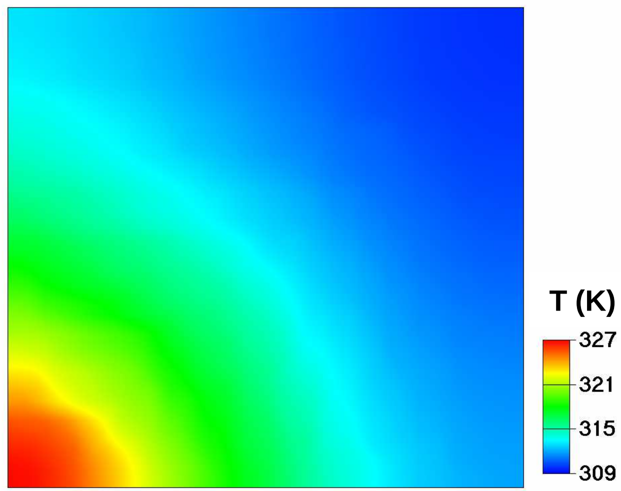
a greater local active region overheating in the planar die

R_{therm} 9.5 K/W



$$R_s \approx (L_{sp}/\sigma_n d_n p)^{-1}$$

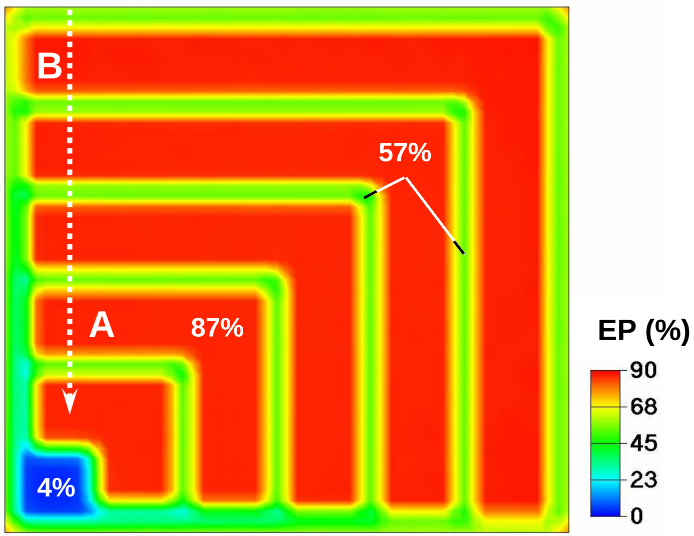
R_{therm} 8.2 K/W



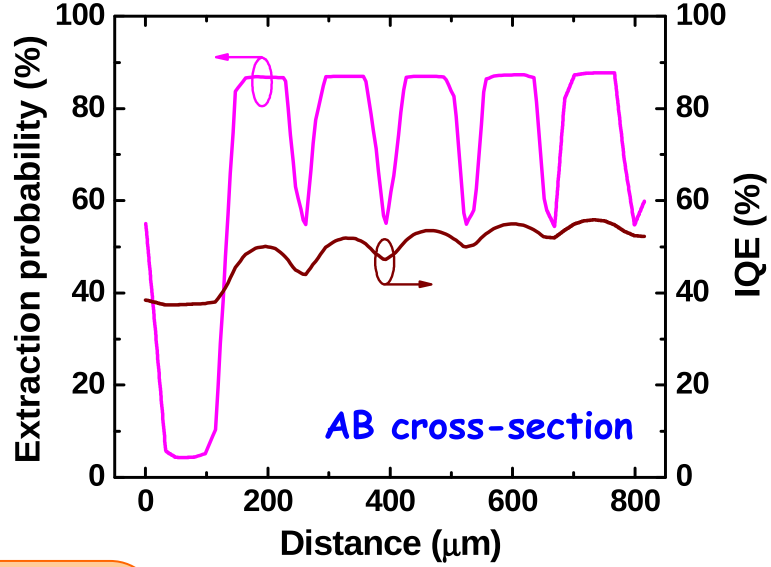
electron concentration in the n-contact layer is ~1×10^{18} cm^{-3} in both dice

Light extraction from the vertical LED die

immersion media: n_r = 1.3

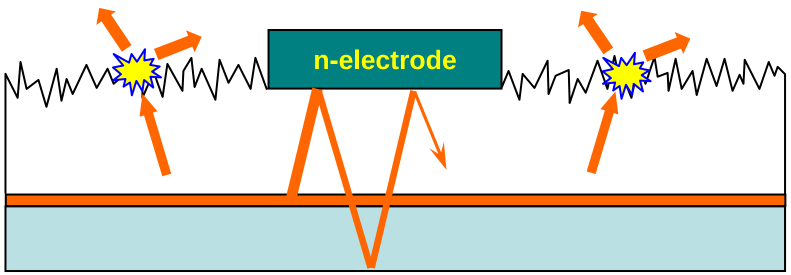


I = 700 mA



probability of light extraction falls down under and next to n-electrode

distribution of extraction probability is nearly independent of current



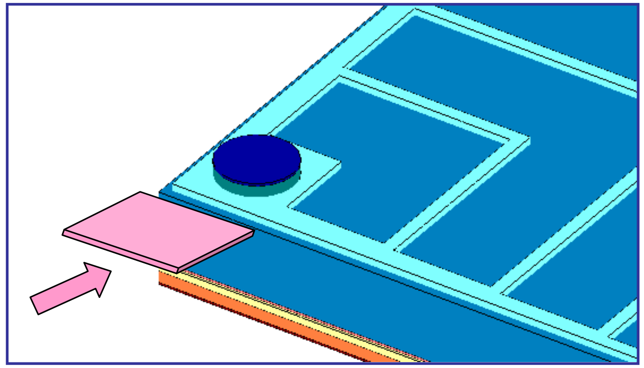
light generated under n-pad is not practically extracted from the die because of incomplete multiple reflection from metallic electrode

Dependence of light extraction efficiency on current for vertical die

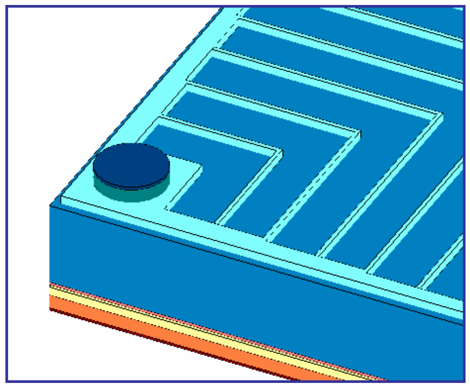
variation of n-contact layer parameters affects weakly the current crowding and, hence, the LEE at ~700-800 mA

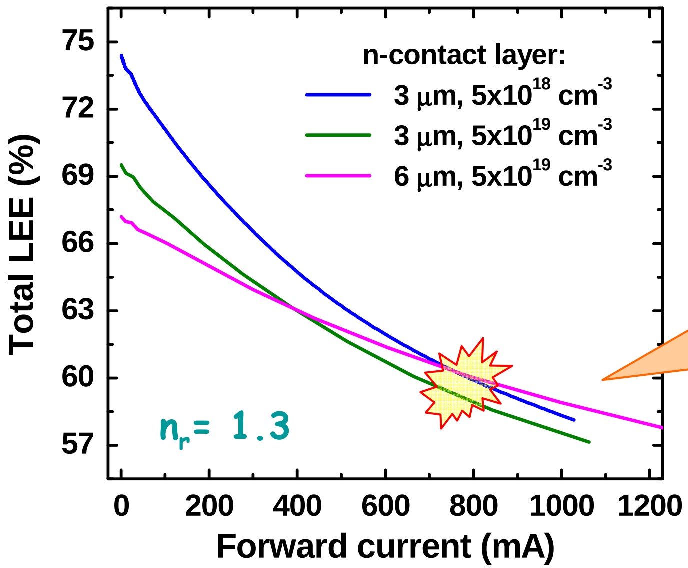
alternative approaches are required

Approach 1: insertion of an insulating layer under the n-pad to avoid parasitic current flow in this region



Approach 2: use of narrower Γ-shaped electrodes with reduced spacing

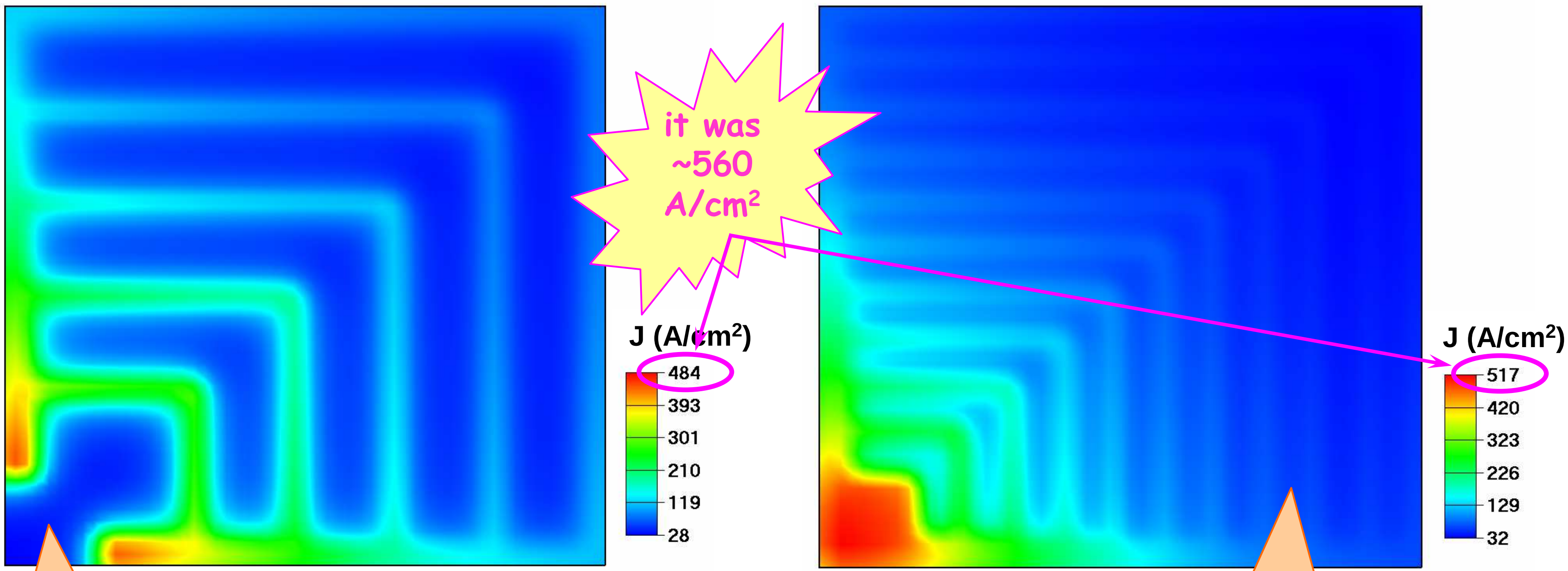




strong dependence of LEE on forward current

Current spreading in vertical LED dice of modified designs

Total current through the diode I = 700 mA



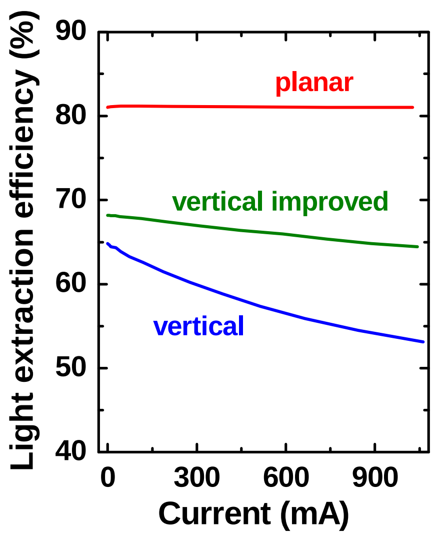
parasitic current flow under the n-pad is partly suppressed

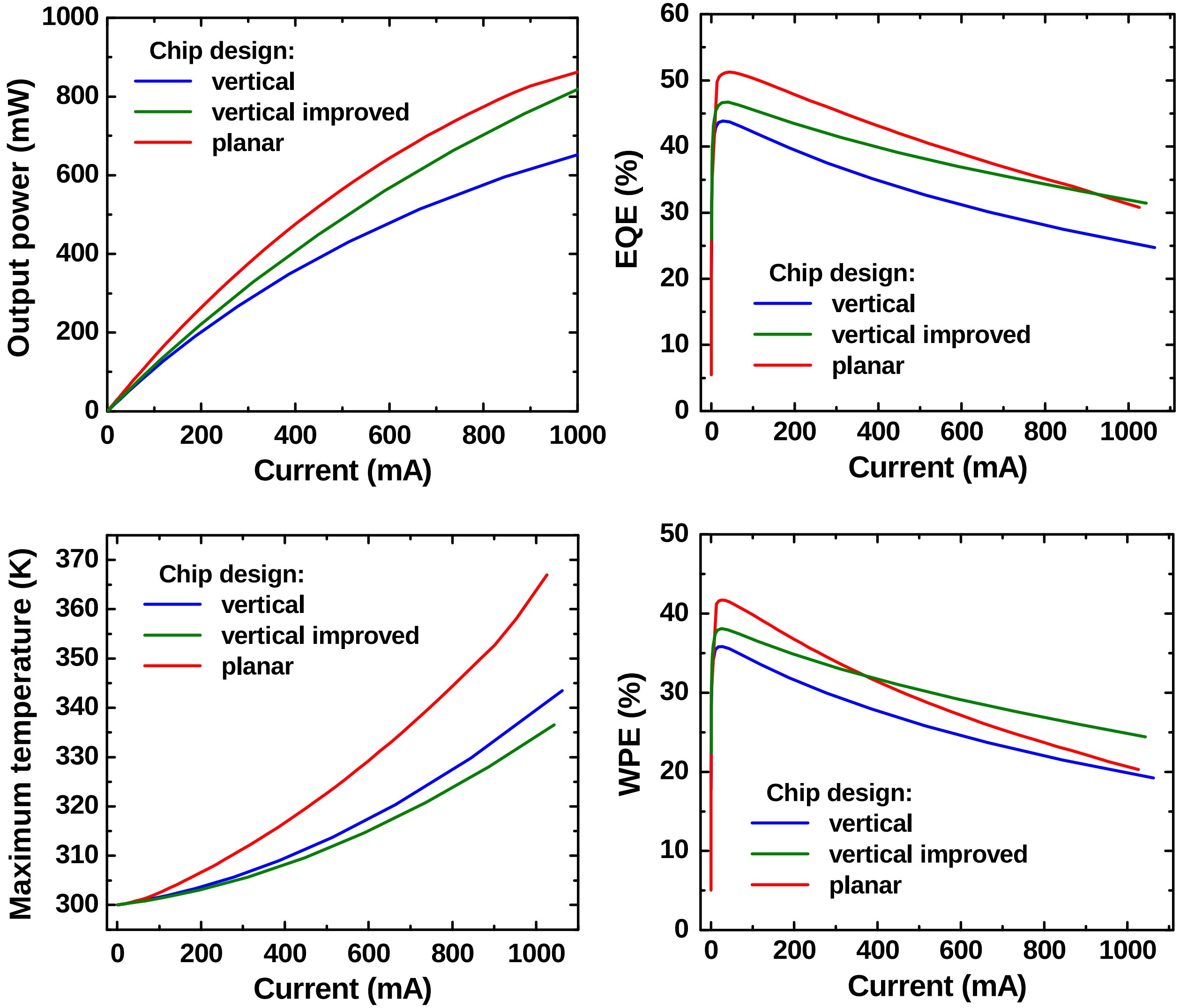
both approaches are found to work well

they are combined in the further consideration

reduction of the current density contrast in the active region

Comparison of characteristics of vertical and planar LEDs





planar LED provides a higher optical power but a stronger droop of both EQE and WPE compared to improved vertical LED

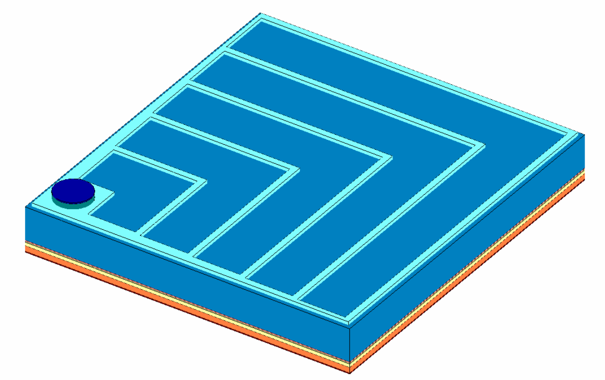
Assessment of general performance of vertical and planar LEDs

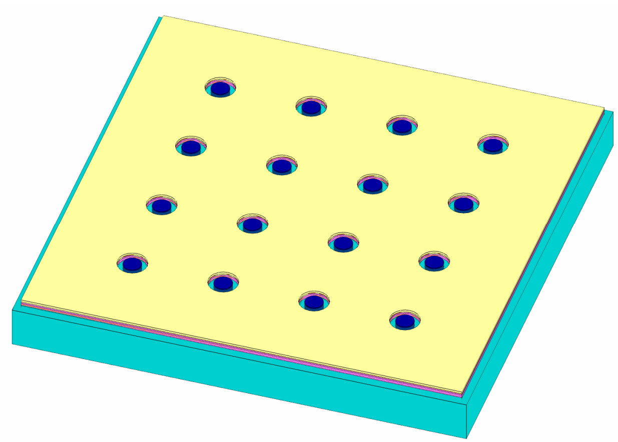
better parameters are marked by yellow color

	Vertical die	Planar die
Operation voltage @ 0.7 A (V)	3.5	4.0
Differential resistance @ 0.7 A (Ω)	0.12	0.70
Light extraction efficiency (%)	70 → 57 @ I = 1.0 A	81 @ all currents
Optical power @ 0.7 A (mW)	530 (640 for improved)	710
External quantum efficiency (%)		
– peak	44 (47 for improved)	51
– @ 1.0 A	25 (32 for improved)	31
Wall-plug efficiency (%)		
– peak	36 (38 for improved)	42
– @ 1.0 A	20 (25 for improved)	20.5
Local active region overheating @ 0.7 A (K)	22 (19 for improved)	36
Current density non-uniformity J_{max}/J_{av} @ 0.7 A	5.3 (4.4 for improved)	10.3
Capability of scaling-up	average	good

degradation-related characteristics ?

Possible directions of further improvement of the LED performance





- using two-pad configuration
- using ITO + highly reflective n-electrodes
- optimization of current-blocking (insulating) film
- optimization of n-electrode geometry

➡ optimization of chip design

- using LED structure with reduced IQE droop, e.g. DHS
- optimization of n-electrode geometry (?)
- improvement of heat-sink (?)

➡ optimization of LED structure